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10/752,703	01/08/2004	Satoshi Kaburaki	02887.0263	8947

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EXAMINER	
GEIB, BENJAMIN P	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 05/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/752,703	KABURAKI ET AL.	
	Examiner	Art Unit	
	Benjamin P. Geib	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Hazm. Fleming
FRITZ FLEMING
Supervisory PRIMARY EXAMINER 5/1/2006
GROUP 2100
AU 2181

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/8/2004 4/21/2004*; 05/12/2004
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-24 have been examined.

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Application on 01/08/2004, Information Disclosure Statement on 04/21/2004, and Information Disclosure Statement on 08/18/2004.

Priority

3. Receipt of papers submitted under 35 U.S.C. 119(a)-(d) is acknowledged; the papers have been placed on record in the file. The certified copies of 2003-003428, filed on 01/09/2003, and 2003-079478, filed on 03/24/2003, have been received and placed on record.

Specification

4. The disclosure is objected to because of the following informalities:

a. Page 8, line 3 – the word "cue" should be changed to –queue--.

Appropriate correction is required.

Claim Objections

5. Claims 2 and 10 are objected to because of the following informalities:

b. Referring to claim 2, the phrase "an other" should be changed to –another--.

c. Referring to claim 10, the phrase "and even when" should be changed to --and, even when--.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. A variety of terms are used in ways contrary to what is known in the art and they are not adequately defined in the specification.

8. Regarding claims 1, 2, 10, 14, 15, and 22:

d. The claims cite the term "processings". This term is indefinite as it is unclear what is meant since the term is not used in a manner known in the art (i.e. the action of processing is not referred to in the plural) and the specification has not adequately defined the term to clarify its meaning.

9. Regarding claims 1-8, 10, 12, and 14-24:

e. The claims cite the term "execution unit". This term is indefinite as it is unclear what is meant since the term is not used in a manner known in the art (i.e. an execution unit is known in the art as a hardware unit that executes an instruction) and the specification has not adequately defined the term to clarify its meaning.

10. Regarding claim 1:

f. Lines 1-2 cite the limitation "A processor which performs data processings including a plurality of execution units". This limitation is indefinite as it is unclear whether "A processor" or "data processings" include a plurality of execution units.

g. Lines 3-5 cite the limitation "a storage which stores data used for processings of the execution units and processing results by the execution units, by each of the execution units". This limitation is indefinite as it is unclear whether the phrase "by each of the execution units" is redundant or is meant to further qualify the limitation.

11. Regarding claim 2:

h. Lines 3-4 cite the limitation "a first storing part which stores data used for the processing of the execution unit prescribed in advance". There is insufficient antecedent basis for this limitation in the claim since there has been no previous mention within the claim of an "execution unit prescribed in advance". Furthermore, it is unclear what the execution unit is prescribed "in advance" of.

12. Regarding claims 6 and 7:

i. The claims cite the phrase "information inherent to the execution units". This phrase is indefinite as it is unclear what is meant since it is not known in the art how information is inherent to an execution unit and the specification has not adequately defined how information can be inherent to an execution unit.

13. Regarding claim 7:

j. Lines 11-12 cite the limitation "a storage controller which transfers contents of the register set used by the other execution unit under suspension or

to be suspended". There is insufficient antecedent basis for this limitation in the claim since there has been no previous mention within the claim of an "other execution unit under suspension or to be suspended".

14. Regarding claim 8:

k. Lines 2-4 cite the limitation "determine whether or not the execution unit determined by said execution unit determination part exists in the register set group". This limitation is indefinite as it is unclear how an "execution unit" can "exist in the register set group". Since, as claimed in claim 7, a register set can exist in the register set group, the above limitation will be interpreted as "determine whether or not the register set used by the execution unit determined by said execution unit determination part exists in the register set group" for the remainder of the examination.

15. Regarding claim 10:

l. Lines 3-6 cite the limitation "when said storage controller is performing an exchanging processing ...". There is insufficient antecedent basis for this limitation in the claim since there has been no previous mention within the claim of a "storage controller".

m. Line 7 cites the limitation "execution unit determination part determines ... without being influenced on the exchanging processing". This limitation is indefinite as it is unclear how an item can be influenced on another item.

16. Regarding claim 11:

n. Lines 1-2 cite the limitation "wherein said storage controller transfers only a value of the register ...". There is insufficient antecedent basis for this limitation in the claim since there has been no previous mention within the claim of a "storage controller".

o. Lines 1-3 cite the limitation "storage controller transfers only a value ... when there is a necessity". This limitation is indefinite as it is unclear whether the storage controller transfers only the stated value or if the storage controller transfers the stated value only when there is a necessity.

17. Regarding claim 12:

p. Lines 1-4 cite the limitation "wherein said storage controller transfers only contents ...". There is insufficient antecedent basis for this limitation in the claim since there has been no previous mention within the claim of a "storage controller".

q. Lines 1-4 cite the limitation "storage controller transfers only contents of the registers ... when it is necessary". This limitation is indefinite as it is unclear whether the storage controller transfers only the contents of the registers or if the storage controller transfers the contents of the registers only when it is necessary.

18. Regarding claim 13:

r. Lines 1-4 cite the limitation "wherein said storage controller transfers contents ...". There is insufficient antecedent basis for this limitation in the claim

since there has been no previous mention within the claim of a "storage controller".

s. Lines 2-3 cite the limitation "transfers contents of the register set to said external register set storage as far as..." This limitation is indefinite as it is unclear what is meant by "as far as". Since the phrase "as far as" appears to be a translation of the idiom "as long as", which is defined as "on the condition that", the limitation will be interpreted as "transfers contents of the register set to said external register set storage on the condition that..." for the remainder of examination.

19. Regarding claim 14:

t. Lines 4-5 cite the limitation "storing data used by processing for the execution unit prescribed in advance into a first storage". There is insufficient antecedent basis for this limitation in the claim since there has been no previous mention within the claim of an "execution unit prescribed in advance". Furthermore, it is unclear what the execution unit is prescribed "in advance" of.

20. Regarding claim 18:

u. The entire claim is replete with grammatical and logical errors and it is unclear what the intended meaning and, thus, metes and bounds, of the claim is.

21. Regarding claim 19:

v. The entire claim is replete with grammatical and logical errors and it is unclear what the intended meaning and; thus, metes and bounds, of the claim is.

22. Regarding claim 23:

w. Lines 11 and 12 cite the limitations "the amount of data of the first storage is increasing tendency" and "the amount of data of the second storage is decreasing tendency", respectively. These limitations are indefinite as it is unclear how an amount of data can be increasing or decreasing tendency.

23. Regarding claim 24:

x. Lines 11 and 12 cite the limitations "the amount of data of the first storage is increasing tendency" and "the amount of data of the second storage is decreasing tendency", respectively. These limitations are indefinite as it is unclear how an amount of data can be increasing or decreasing tendency.

24. All claims rejected by 35 U.S.C. 112, second paragraph, that have not been specifically addressed above are rejected on the basis of dependence.

Claim Rejections - 35 USC § 102

25. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

26. Claims 1-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Parady, U.S. Patent No. 5,933,627.

27. Referring to claim 1, Parady has taught a processor which performs data processings including a plurality of execution units, comprising:

a storage *[instruction buffers; Fig. 3, components 102, 104, 106, & 108]* which stores data used for processings of the execution units and processing results by the execution units, by each of the execution units *[column 3, lines 36-43]*;

a data processing part *[execution units and register files; Fig. 3, components 41, 48, & 50]* configured to acquire data of the execution units from said storage to perform the processings, and configured to output the processing results in said storage *[column 3, lines 19-25, 39-43]*;

an execution unit judgement part *[dispatch unit; Fig. 3, component 28]* configured to determine whether or not said storage holds data used for the processings of a certain execution unit, and whether or not said storage has a vacant region capable of storing the processing result of the certain execution unit *[column 3, lines 11-18]*; and

an execution unit determination part *[thread switching logic; Fig. 3, component 112]* which determines an execution unit to be processed next among said plurality of execution units, based on a result judged by said execution unit judgement part *[column 3, lines 57-65]*.

28. Referring to claim 2, Parady has taught the processor according to claim 1, wherein said storage includes:

a first storing part *[thread 0 instruction buffer ; Fig. 3, component 102]* which stores data used for the processing of the execution unit prescribed in advance *[column 3, lines 36-43]*; and

a second storing part *[thread 1 instruction buffer; Fig. 3, component 104]* which stores the processing result obtained by performing the processings of the corresponding execution unit by using data acquired from said first storage, and stores data used by an other execution unit using the processing result by the corresponding execution unit *[column 3, lines 36-43]*,

wherein said execution unit judgement part *[dispatch unit]* judges whether or not said first storing part holds data used for the processing of the execution unit, and whether or not said second storage part has the vacant region storing the processing result of the execution unit *[column 3, lines 11-18]*.

29. Referring to claim 3, Parady has taught the processor according to claim 2, further comprising

a priority setting part *[thread field; Fig. 4, component 118]* configured to set priorities to said plurality of execution units *[column 4, lines 19-30]*,

wherein said execution unit determination unit determines the execution unit to be started up, based on the priorities set by said priority setting unit *[column 4, lines 19-30]*.

30. Referring to claim 4, Parady has taught the processor according to claim 3 further comprising a start-up frequency measuring part configured to measure start-up frequencies of said plurality of execution units, wherein said priority setting part sets the priorities based on the start-up frequency measured by said start-up frequency measuring part *[column 4, lines 31-41]*.

31. Referring to claim 5, Parady has taught the processor according to claim 3, wherein when a first execution unit is being started up, said execution unit determination part holds data used for a second execution unit with a priority higher than said first execution unit, and suspends operation of said first execution unit to start up said second execution unit when said second storage has the vacant region to store the processing result by said second execution unit *[column 4, lines 42-52]*.

32. Referring to claim 6, Parady has taught the processor according to claim 2, wherein said data processing part includes:

a register set group *[integer register files; Fig. 3, component 48]* which has a plurality of register sets including all of information inherent to the execution units *[column 3, lines 44-49]*;

a register set selector which selects the register set used by the execution units determined by said execution unit determination part *[Since there are multiple register sets, it is inherent that there is a selector to select one of them.]*; and

an operation processing part *[execution units; Fig. 3, component 41]* configured to perform processing of the execution unit decided by said execution unit determination part by using the register set selected by said register set selector *[column 3, lines 19-25, 39-43]*.

33. Referring to claim 7, Parady has taught the processor according to claim 2, further comprising:

a register set group *[main integer register files; Fig. 6, component 184]* which has a plurality of register sets including all of information inherent to the execution units *[column 5, lines 24-29]*;

a register set selector which selects the register set used by the execution units determined by said execution unit determination part *[Since there are multiple register sets, it is inherent that there is a selector to select one of them.]*;

an operation processing part *[integer execution unit; Fig. 6, component 156]* configured to perform processing of the execution unit decided by said execution unit determination part by using the register set selected by said register set selector *[column 3, lines 19-25]*

an external register set storage *[shadow register files; Fig. 6, component 186]* capable of storing contents of an arbitrary register set included in said register set group *[column 5, lines 24-36]*; and

a storage controller *[data switch; Fig. 7, component 192]* which transfers contents of the register set used by the other execution unit under suspension or to be suspended, included in the register set group, to said external register set storage, when contents of the register set used by the execution unit is stored in said external register set storage, and transfers data from said external register set storage to the register set *[column 5, lines 38-43]*.

34. Referring to claim 8, Parady has taught the processor according to claim 7, further comprising

a hit determination part *[grouping logic; Fig. 6, component 184]* configured to determine whether or not the execution unit determined by said execution unit determination part exists in the register set group *[column 5, lines 24-36]*,

wherein said register set selector selects the register set from said register set group when said hit determination part determines that the register set used by the execution unit exists in said register set group, and selects the register set which holds data transferred from said external register set storage when said hit determination part determines that the register set does not exist in said register set group *[column 5, lines 24-36]*.

35. Referring to claim 9, Parady has taught the processor according to claim 8, further comprising

a retreating register set determination part *[data switch; Fig. 7, component 192]* configured to select the register set to retreat into said external register set storage from said register set group when said hit determination part determines that the register set does not exist in said register set group, wherein said storage controller transfers contents of the register set selected by said retreating register set determination part to said external register set storage *[column 5, lines 38-43]*.

36. Referring to claim 10, Parady has taught the processor according to claim 6, wherein said execution unit determination part *[thread switching logic]* determines the execution unit by taking into consideration the judgement result by said execution unit judgement part, and, even when said storage controller is performing an exchanging processing of the register sets between said register set group and said external

register set storage, determines the execution unit capable of executing the processings without being influenced on the exchanging processing *[column 3, lines 57-65].*

37. Referring to claim 11, Parady has taught the processor according to claim 6, wherein said storage controller transfers only a value of the register changed among said register set group, to said external register set storage when there is a necessity to update contents stored in said external register set storage *[When a storage controller transfers data it has considered the transfer necessary. Therefore, it is inherent that the transfer is done when there is a necessity].*

38. Referring to claim 12, Parady has taught the processor according to claim 6, wherein said storage controller transfers only contents of the registers changed by executing an other execution unit from said external register set storage to said register set group, when it is necessary to transfer data from said external register set storage to said register set group *[When a storage controller transfers data it has considered the transfer necessary. Therefore, it is inherent that the transfer is done when there is a necessity].*

39. Referring to claim 13, Parady has taught the processor according to claim 6, wherein said storage controller transfers contents of the register set to said external register set storage as far as the same register set as the register set stored in said external register set storage does not exist in said register set group *[column 5, lines 38-43].*

40. Claims 14-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Nemirovsky et al., U.S. Patent No. 6,477,562 (Herein referred to as Nemirovsky).

41. Referring to claim 14, Nemirovsky has taught an arithmetic operation processing method, comprising:

executing processings by each of execution units which executes time-sharing processings for a certain data processing *[column 7, lines 39-50]*;

storing data used by processing for the execution unit prescribed in advance into a first storage *[source registers for stream A; column 7, lines 12-16]*;

storing the processing result obtained by processing of the corresponding execution unit by using data acquired from said first storage into a second storage *[destination registers for stream A; column 7, lines 12-16]*, and storing data used by processings of an other execution unit using the stored processing result by the corresponding execution unit *[column 7, lines 12-16]*;

judging whether or not said first storage holds data using to the processings of the execution unit, and whether or not said second storage has a vacant region to store the processing result of the execution unit *[instruction scheduler schedules stream A after determining source and destination register are available; column 7, lines 29-42]*; and

determining the execution unit to be started up next among said plurality of execution units *[using the priority controller; column 6, lines 9-24, 50-60]*.

42. Referring to claim 15, Nemirovsky has taught a processor, comprising:

a data processing part *[function units; Fig. 2, component 207-210]* configured to execute processings by each of execution units which execute time-sharing processings for a certain data processing *[column 7, lines 39-50]*;

a plurality of storages *[register files]* which stores data used by the execution unit to be executed by said data processing part, or an execution result of data used by the execution unit to be executed by said data processing part *[column 7, lines 12-16]*; and

a priority determination part *[priority controller; Fig. 2, component 9]* configured to determine priorities of the execution units using data stored in the storages based on the amount of data stored in said plurality of storages *[column 6, lines 9-24, 50-60]*.

43. Referring to claim 16, Nemirovsky has taught the processor according to claim 15, wherein said priority determination part determines a higher priority for the execution unit receiving data to be processed from said storage, as the amount of data stored by a certain storage is larger *[column 10, line 47 – column 11, line 2]*.

44. Referring to claim 17, Nemirovsky has taught the processor according to claim 15, wherein said priority determination part determines a lower priority for the execution unit storing the execution result in said storage, as the amount of data stored by a certain storage is larger *[column 10, line 47 – column 11, line 2]*.

45. Referring to claim 18, Nemirovsky has taught the processor according to claim 16, wherein as compared a first case where the amount of data stored in the storage receiving data to be processed by a certain execution unit is in an increasing tendency with a second case where data stored in the storage receiving data to be processed by the certain execution unit is in a decreasing tendency, even if the amount of data stored

in said storage in said first case is equal to the amount of data stored in said storage in said second case, the priority of the execution unit receiving data to be processed from said storage in said second case is set higher than that of the execution unit in said first case *[column 10, line 47 – column 11, line 2]*.

46. Referring to claim 19, Nemirovsky has taught the processor according to claim 17, wherein as compared a first case where the amount of data stored in the storage storing the execution result by a certain execution unit is in an increasing tendency with a second case where the amount of data stored in the storage storing the execution result by the certain execution unit is an decreasing tendency, even if the amount of data stored in said storage in said first case is equal to the amount of data stored in said storage in said second case, the priority of the execution unit storing the execution result in the storage in said first case is set higher than that of the execution unit in the second case *[column 10, line 47 – column 11, line 2]*.

47. Referring to claim 20, Nemirovsky has taught the processor according to claim 15, wherein said priority determination part sets the highest priority for the execution unit which receives data to be processed from a certain storage when determined that the data amount stored by said certain storage exceeds a limit of memory capacity of said certain storage *[column 10, line 47 – column 11, line 2]*.

48. Referring to claim 21, Nemirovsky has taught the processor according to claim 15, wherein said priority determination unit sets the lowest priority for the execution unit which receives data to be processed from a certain storage when determined that the

data amount stored by said certain storage exceeds a limit of memory capacity of said certain storage *[column 10, line 47 – column 11, line 2]*.

49. Referring to claim 22, Nemirovsky has taught a priority determination method, comprising:

executing processing by each of execution units which executes time-sharing processings for a certain data processing *[column 7, lines 39-50]*;

storing data used by an execution unit to be executed or an execution result by the execution unit, into a plurality of storages *[register files; column 7, lines 12-16]*; and

determining a priority *[using the priority controller; Fig. 2, component 9]* of the execution unit using data stored in said storages based on the data amount stored in said plurality storages *[column 6, lines 9-24, 50-60]*.

50. Referring to claim 23, Nemirovsky has taught the processor according to claim 16,

wherein the execution units include a first execution unit *[stream A]* and a second execution unit *[stream B] [column 6, lines 24-40]*,

wherein the plurality of storages include a first storage to store data used by the first execution unit *[register file for stream A]* and a second storage to store data used by the second execution unit *[register file for stream B] [column 7, lines 12-16]*,

wherein the priority determination part sets the priority of the first execution unit lower than the second execution unit, if the following conditions are fulfilled:

(a) the amount of data of the first storage is equal to that of the second storage *[column 10, line 47 – column 11, line 2]*;

(b) the amount of data of the first storage is increasing tendency *[column 10, line 47 – column 11, line 2]*; and

(c) the amount of data of the second storage is decreasing tendency *[column 10, line 47 – column 11, line 2]*.

51. Referring to claim 24, Nemirovsky has taught the processor according to claim 17,

wherein the execution units include a first execution unit *[stream A]* and a second execution unit *[stream B] [column 6, lines 24-40]*,

wherein the plurality of storages include a first storage to store the execution result of the first execution unit *[register file for stream A]* and a second storage to store the execution result of the second execution unit *[register file for stream B] [column 7, lines 12-16]*,

wherein the priority determination part sets the priority of the first execution unit higher than the second execution unit, if the following conditions are fulfilled:

(a) the amount of data of the first storage is equal to that of the second storage *[column 10, line 47 – column 11, line 2]*;

(b) the amount of data of the first storage is increasing tendency *[column 10, line 47 – column 11, line 2]*; and

(c) the amount of data of the second storage is decreasing tendency *[column 10, line 47 – column 11, line 2]*.

Conclusion

52. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

53. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ang, U.S. Patent No. 6,918,116, has taught a system for thread scheduling to run in parallel with a main processor.

Sakuma et al., U.S. Patent No. 5,148,542, has taught a processor for processing a plurality of tasks.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Benjamin P Geib
Examiner
Art Unit 2181

ftz m. fleming

FRITZ FLEMING
Supervisory PRIMARY EXAMINER 5/1/2006
GROUP 2100
AU 2181